HYBRID CMOS/NANOELECTRONIC CIRCUITS:

(II) LOW-LEVEL DEVELOPMENT OF HYBRID CIRCUITS

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Outline

- Circuit level basics and challenges of hybrid CMOS/nano circuits (Dima)
- Nanoelectronic device modeling and fabrication (Garrett)
- Majority-logic and NDR device options for hybrid circuits (Garrett)

Major circuit-level challenges

1) CMOS/nano interface

2) Homogeneous nanolayer

3) Low device functionality

4) Defect tolerance

← efficient solution: CMOL (part I)
quantitatively discussed in part III

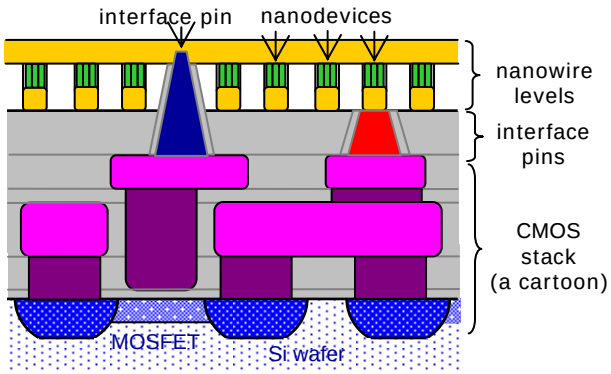
← Xbar implications on circuit design?

← discussed in part I, desired I-V on the example of basic operation in Xbars, detailed models and scaling issues

← part III

in this part

Reminder from part I:
circuits = nano Xbar + CMOS



Homogeneous nanoXbar

To deal with homogeneity

- At least bistable nanodevice
- CMOS circuitry support for programmability

Topologically Xbars are

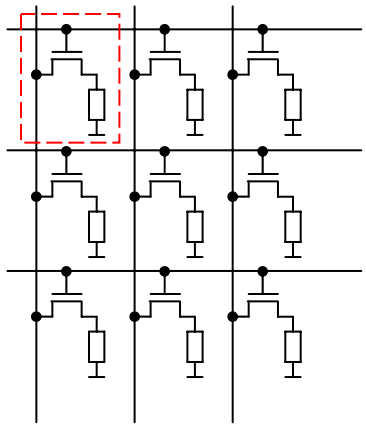
- Enabling for neuromorphic networks
- Natural for memory apps
- Not obvious for digital logic

  but at least include all memory circuitry to support programmability

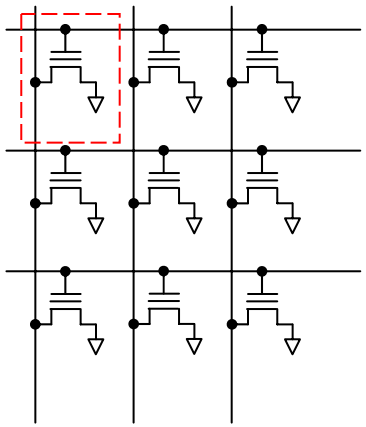
Resistive Xbar Topology for Memory Apps

similar topology to conventional memories but no access transistor → specific properties of nanodevice

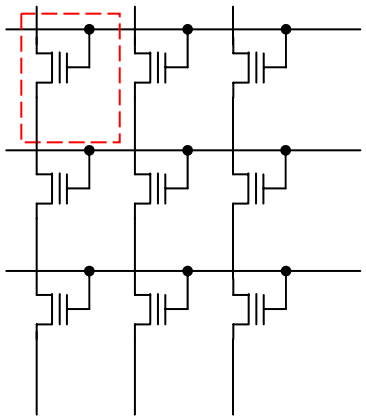
this tutorial



DRAM, FeRAM (1T1C), RRAM, PRAM, MRAM, (1T1R), TFT-LCD etc.

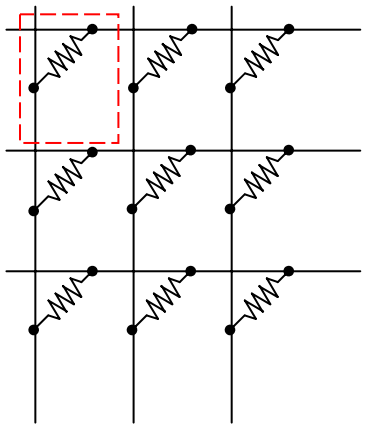


Flash NOR (1FGT), FeRAM (1T)



Flash NAND (1FGT)

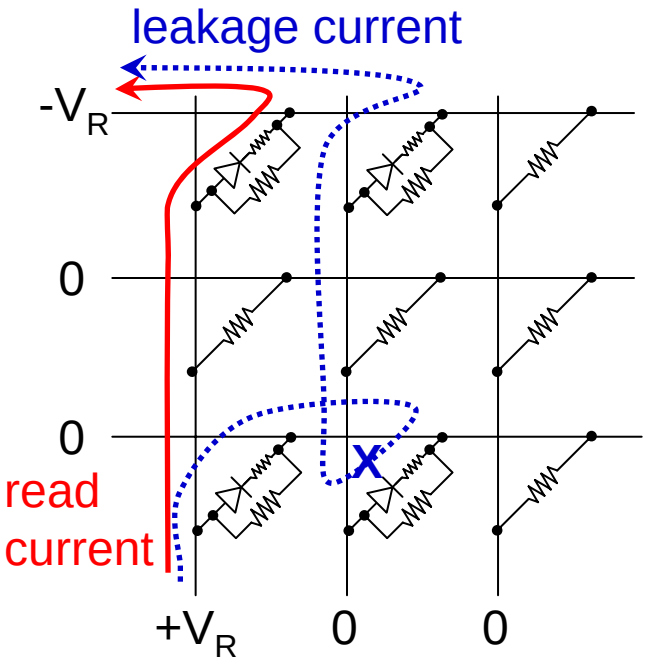
CMOS >45 nm

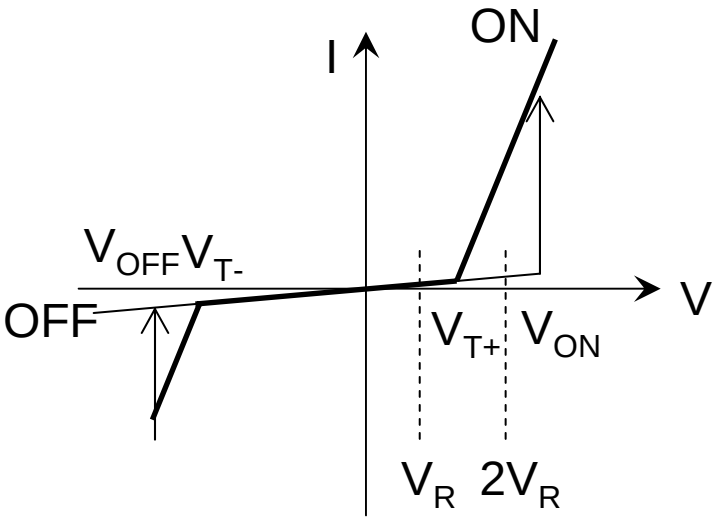


Resistive Xbar (0T1R)

nano <10 nm

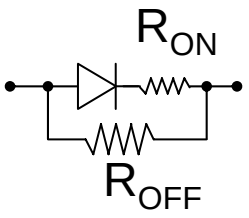
Minimum device functionality: Requirements for read operation



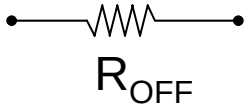


(#1) Diode like non-linearity $|V_{T-}| > V_R$

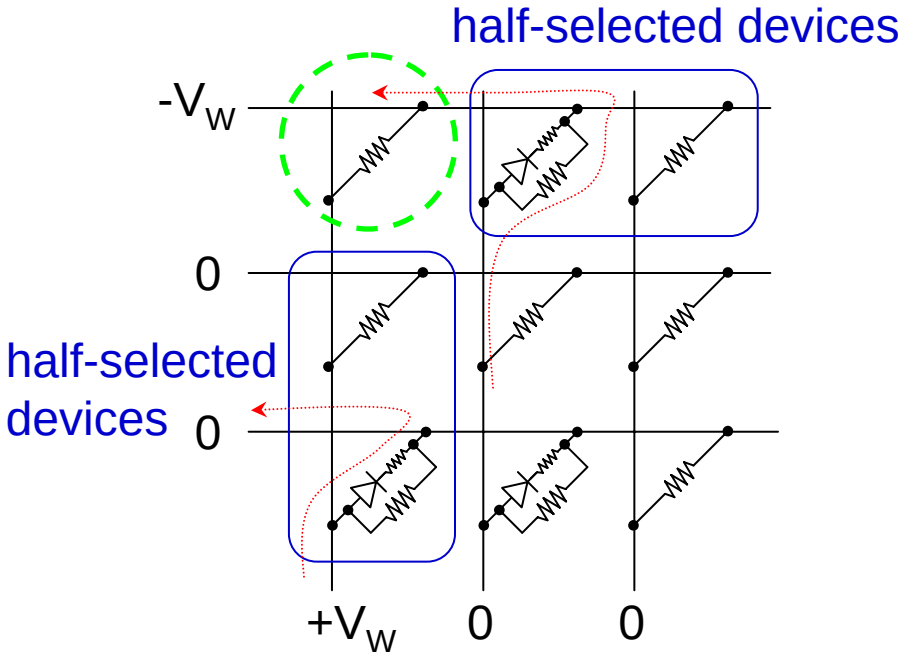
ON state:

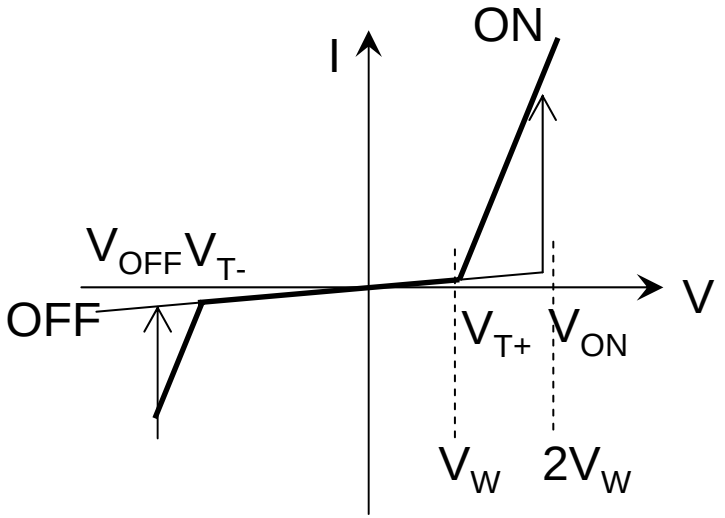


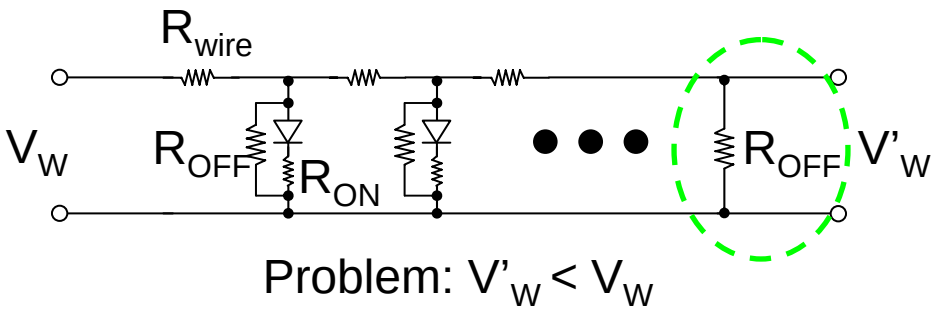
OFF state:



Minimum device functionality: Requirements for write operation







Problem: $V'_W < V_W$

- Float nanowires? but huge RC, bad tolerance to transients
- Potentially much worse for forming step if any!

(#2) Resistance $R_{wire} << R_{ON}(V_{T+})$
e.g. forward-bias nonlinearity $V_{T+} > V_W$