

Aluminum oxide layers as possible components for layered tunnel barriers

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(Received 14 January 2004; accepted 26 April 2004)

We have studied transport properties of Nb/Al/AIO_x/Nb tunnel junctions with ultrathin aluminum oxide layers formed by (i) thermal oxidation and (ii) plasma oxidation, before and after rapid thermal postannealing of the completed structures at temperatures up to 550 °C. Postannealing at temperatures above 300 °C results in a significant decrease of the tunneling conductance of thermally grown barriers, while plasma-grown barriers start to change only at annealing temperatures above 450 °C. Fitting the experimental *I-V* curves of the junctions using the results of the microscopic theory of direct tunneling shows that the annealing of thermally grown oxides at temperatures above 300 °C results in a substantial increase of their average tunnel barriers height, from ~1.8 eV to ~2.45 eV, versus the practically unchanged height of ~2.0 eV for plasma-grown layers. This difference, together with high endurance of annealed barriers under electric stress (breakdown field above 10 MV/cm) may enable all-AIO_x and SiO₂/AIO_x layered “crested” barriers for advanced floating-gate memory applications. © 2004 American Institute of Physics.
 [DOI: 10.1063/1.1763229]

I. INTRODUCTION

Calculations^{1–3} indicate that tunnel conductance of layered barriers, in particular those with “crested” potential profile peaking in the middle, may be much more sensitive to the applied voltage than that of the uniform layers.⁴ This sensitivity, if combined with high endurance to electric stress, may be used in advanced floating-gate memories, including fast and scalable random access memories,⁵ fast single- and few-electron memories,^{6,7} and ultradense data storage systems,¹ as well as for improvement of the usual nonvolatile (e.g., “flash”) memories.^{8,9} However, finding an appropriate combination of materials for crested barrier layers presents a challenge. Indeed, numerous experiments (for a review see, e.g., Ref. 10) indicate that just a few known CMOS-compatible materials may combine the barrier height sufficient for thermionic current suppression at room temperature (above ~1.5 eV), with the necessary high breakdown field (above 10 MV/cm), and negligible trap-assisted tunneling. To our knowledge (see also the recent theoretical calculations),¹¹ the list of such candidate materials is essentially limited to: (i) silicon dioxide, (ii) low-trap-density silicon nitride that may be grown using special methods,^{12,13} and (iii) aluminum oxides grown by a variety of methods including notably thermal¹⁴ and plasma¹⁵ oxidation.

The goal of this paper is to show that the aluminum oxides represent a good material choice for fabrication of crested barriers. Experimental measurements of the most important parameter in this context, the average tunnel barrier height $\langle U \rangle$, have been reported for aluminum oxide layers in quite a few publications. Unfortunately, the cited values of

$\langle U \rangle$ are scattered rather broadly: for thermally grown oxides, most results are in the range from 1.7 to 2.5 eV (see, e.g., Refs. 16–22), but values as low as 1.2 eV,²³ and as high as 4.75 eV,²⁴ or even 20 eV,²⁵ have also been derived from the data. Similarly, for plasma-grown layers, most reported values of $\langle U \rangle$ are in the range from 1.7 to 2.3 eV (see, e.g., Refs. 24, 26–30),³¹ but numbers as high as 3.6 eV have also been claimed.²⁹ The published results for the apparent barrier asymmetry, $\Delta U \equiv U_{\max} - U_{\min}$, are scattered even more, from a few tenths of eV all the way up to 6 eV,²⁴ and the only apparent consensus is that the barrier is always higher at the top (counterelectrode) interface. Probably, the most important source of these differences are peculiarities of the film fabrication, including the substrate temperature (that has not always been carefully monitored) and the counterelectrode material. However, some result scattering may be also attributed to the variety of techniques used for barrier height measurement, including *I-V* curve fitting,^{16,17,19–22,24,25,27–30} photoelectric effect,^{18,20,26} and ballistic electron emission spectroscopy.²³ Some of these methods may give rather inaccurate results. For example, as has been shown in our recent work,²² fitting of *I-V* curves of aluminum oxide barriers with Wentzel-Kramer-Brillouin (WKB) approximation results may lead to substantial errors, since such barriers are rather thin and sharp. These errors may be dramatically increased if low-*V* expansions of WKB formulas^{32,33} are used, as this procedure is highly vulnerable to minor additional currents due to inelastic (e.g., trap-assisted) tunneling—see, e.g., Fig. 5 and its discussion below. Our experience shows that fitting the slope of the “Fowler-Nordheim plot” ($\ln I$ vs $1/V$) of high-*V* data may also lead to very substantial errors. The experimental information on the effective mass of the tunneling electrons is even more limited (see the discussion below).

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One more motivation for additional experimentation was to study the effects of thermal postannealing of tunnel junctions. It was noticed previously that thermal annealing may improve tunneling magnetoresistance of junctions between magnetic layers.^{34–40} Some changes in the average barrier height $\langle U \rangle$ at annealing were noticed in Refs. 34, 36, and 38–41. However, the change was typically small (in many cases, due to low annealing temperature), so that no definite conclusions could be drawn even about the sign of the effect. Moreover, the uncertainty of the results, obtained using the WKB expansion,^{32,33} is probably comparable with the barrier change itself. Because of this reason, in this work we have carried out detailed studies of tunnel barriers grown by thermal and plasma oxidation of aluminum, and rapid postannealed at various temperatures.

II. SAMPLE FABRICATION AND EXPERIMENTAL TECHNIQUES

The oxide layers have been grown on 2 in. silicon wafers ($\rho \approx 10 \Omega \text{ cm}$) covered by 500 nm of thermally grown SiO_2 , in a cryopumped vacuum system with a base pressure close to 2×10^{-7} torr, as components of standard Nb-trilayer junctions.⁴² First, a 150-nm-thick niobium base film has been deposited using dc-magnetron sputtering at a rate of 1.6 nm/s. Then, without breaking the vacuum, a 10-nm-thick aluminum film has been deposited by the same method at a lower speed (0.5 nm/s). It is well known⁴² that at these conditions aluminum wets the niobium surface, forming a smooth uniform coating.

After that, the aluminum film has been oxidized either thermally (at room temperature) or in oxygen plasma. In the former case, a well-monitored amount of ultra-high-purity (semiconductor-grade) oxygen has been let into the vacuum chamber for a certain time. The same gas has been used for the plasma oxidation, but in this case a 13.56 MHz source has been connected, via a tuned resonant circuit, to a dc-insulated copper plate on which the substrate had been mounted. This has resulted in a 50 W rf plasma discharge and wafer dc self-biasing to approximately -80 V relative to the ground (vacuum chamber walls). The wafer has been kept at room temperature by its thermal anchoring to the water-cooled copper plate.

After the oxidation, the chamber has been pumped down to the base pressure and a niobium 100-nm-thick counterelectrode has been deposited *in situ* in the same way as the base electrode. The fabrication had been completed by sample patterning into junctions of various area A (3×3 , 30×30 , and $300 \times 300 \mu\text{m}^2$) using optical lithography with PMMA resist and reactive ion etching in SF_6 plasma. Here, the same photoresist mask was first used for the counterelectrode shape definition using RIE, and later for a lift-off of a sputtered 150-nm-thick SiO_2 insulation layer from the junction surface. The lift-off has opened contacts of junction counterelectrodes with the following thicker niobium wiring layer.

After initial characterization, a few $5 \times 5 \text{ mm}^2$ chips from each wafer have been subjected to rapid thermal annealing in inert atmosphere (either Ar or N_2). Direct current I - V measurements of both as-oxidized and annealed junctions have

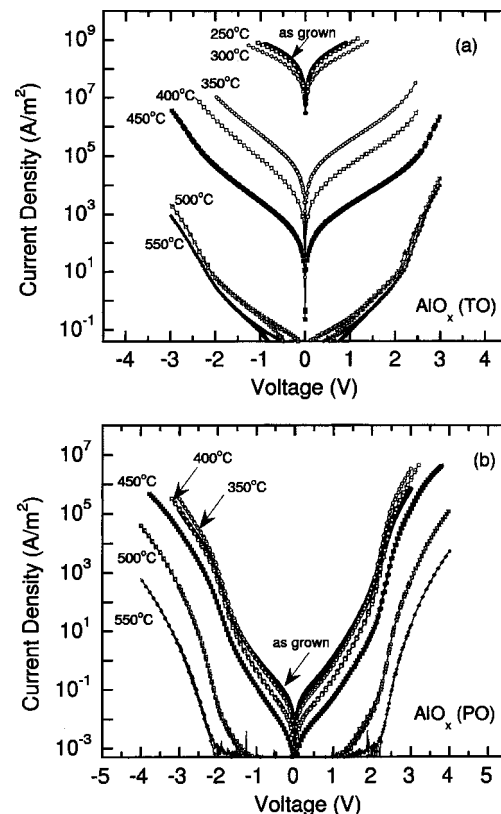


FIG. 1. Experimental current density J as a function of the applied dc voltage V for Nb/Al/ AlO_x /Nb junctions with (a) thermally grown (Crest 5) and (b) plasma-grown (Crest 19) oxide layers, before and after the rapid thermal anneals at indicated temperatures, as measured at 4.2 K. The noisy flattening of the lower curve in panel (b) at small voltages is due to leakage of our measurement setup at $I \leq 10^{-13} \text{ A}$.

been carried out at both room and helium (4.2 K) temperatures, using a special low-noise, high-sensitive setup. Voltage sweeps with gradually growing amplitude were used to characterize transport up to the very onset of hard breakdown.

III. EXPERIMENTAL RESULTS AND THEORETICAL FITTING

Here we focus on comparing the results from two representative wafers: “Crest 5” (thermal oxidation for 40 min at 100 Torr) and “Crest 19” (plasma oxidation for 10 min at 15 mTorr), both postannealed at temperatures up to 550°C .⁴³ The junctions, both before and after postannealing, were highly reproducible, with the rms on-chip (junction-to-junction) variation of low-voltage conductance from as low as 0.8% (considerably better than any published results we are aware of) to $\sim 20\%$ (comparable with reported results—see, e.g., Ref. 44).

Figure 1 shows I - V curves of representative junctions from these two wafers, both before and after postannealing at various temperatures. (These data have been taken at helium temperature; however, the increase of temperature to 300 K changes the current only slightly—see Fig. 2). First of all, one can see that the annealing above $\sim 300^\circ\text{C}$ leads to a considerable improvement of the junction quality: the hard breakdown voltage V_b increases, and the I - V curves show virtually no hysteresis or “soft breakdown,” up to V_b . (For

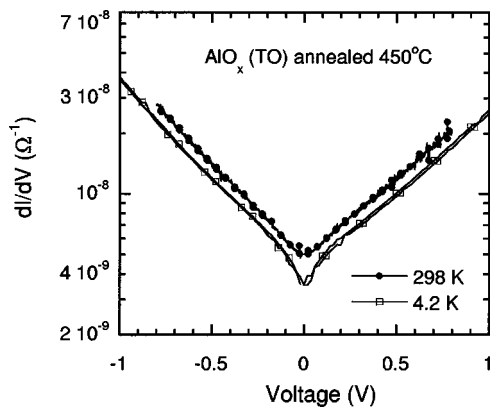


FIG. 2. The nonlinear “dynamic” conductance $G(V) \equiv dI/dV$ of a typical 450 °C-annealed sample from wafer Crest 5, measured at liquid helium and room temperatures.

thermally grown oxides annealed at ~ 500 °C and beyond, the hysteresis appears again, though V_b continues to grow.) More quantitatively, the charge to breakdown, measured at room temperature for samples annealed at 450 °C, stays above 10^5 C/cm² (i.e., a few orders of magnitude higher than the level typical for industrial grade SiO₂ barriers¹⁴ until ~ 2.1 V for both Crest 5 and Crest 19 samples.

However, our most important observation is a dramatic difference between the effects of annealing temperature upon the thermally grown and plasma-grown oxides: while the low-voltage conductance of the former junctions drops sharply starting above ~ 300 °C and decreases by almost six orders of magnitude by 450 °C,⁴⁵ the reduction in the latter barriers is minor (below two orders of magnitude) until the annealing temperature has been raised to ~ 500 °C. In order to give at least a phenomenological interpretation of this effect, we have used theoretical fits to extract essential tunnel barrier parameters of the AlO_x layers.

The shape of I - V curves of the samples (Fig. 1), and their very weak temperature dependence (Fig. 2) are consistent with the assumption of direct tunneling of electrons through the barrier.⁴⁶ [This conclusion is also supported by the results of high-resolution microscopy (Fig. 3) and electron energy loss spectroscopy (Fig. 4) of the annealed samples, showing a well-defined oxide layer with sharp interfaces with both base and counterelectrodes.] This is why we have fitted our experimental data with results of a “microscopic” (non-WKB) theory of such tunneling. Our general computer algorithm is based on the joint solution of the one-dimensional (1D) Schrödinger equation (using the transfer-matrix technique) and Poisson equation for tunneling electrons.⁴⁷ However, we have found that the barrier shape modification by the charge of tunneling electrons is very small. The exclusion of the Poisson solver from the code makes it very fast: simulation of one I - V curve in ~ 100 points with a few-percent accuracy takes about 1 min on a single-processor workstation. The code has been checked on the results for SiO₂ layers described in Ref. 48, and gave similar results to those of the theoretical calculations in that seminal paper.

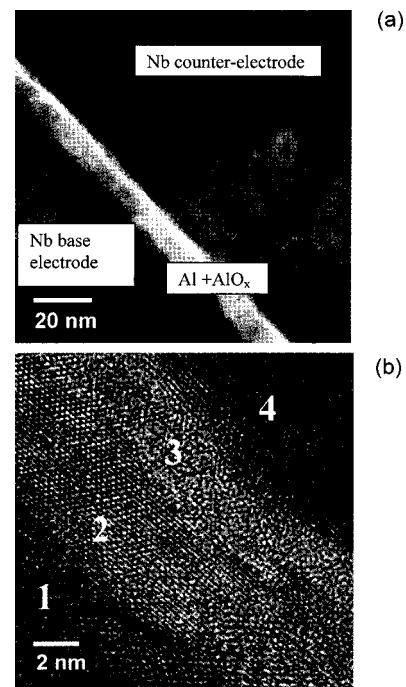


FIG. 3. (a) High-resolution transmission-electron-microscope image of a 450 °C postannealed sample from wafer Crest 5 and (b) magnified part of the layered structure with the position of the electron energy loss spectroscopy spectra indicated.

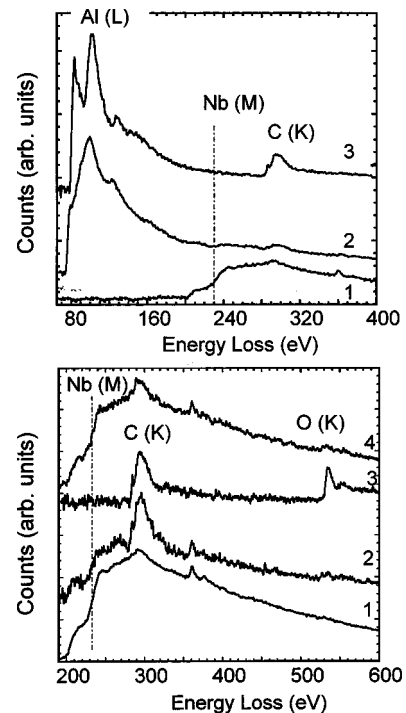


FIG. 4. Results of the electron energy loss spectroscopy for two energy ranges from the positions indicated in Fig. 3(b): (1) Nb base electrode, (2) the middle of Al layer, (3) AlO_x layer, and (4) Nb counterelectrode. The spectra are background subtracted, and corrected for multiple scattering contributions. The carbon K -edge present in all the spectra stems from the carbon build-up during the spectrum acquisition and is not a feature of the sample structure.

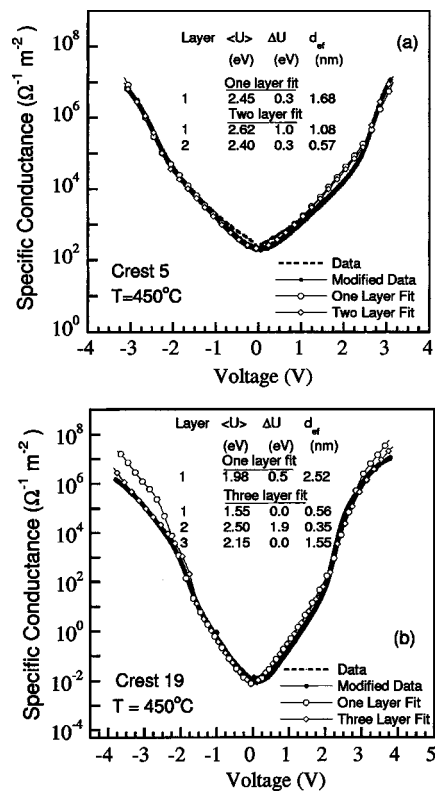


FIG. 5. Fitting of the specific dynamic conductance $g(V) \equiv A^{-1}dI(V)/dV$ of postannealed (450 °C) junctions with (a) thermally grown and (b) plasma-grown barriers with microscopic theory of direct tunneling. Dashed lines show raw data, lines with solid points—the data corrected for trap-assisted tunneling, curves with open circles show the best fits with one-layer (trapezoidal) model, while those with open diamonds for more complex potential profiles. The fitting parameters [the average barrier height $\langle U \rangle$, asymmetry ΔU , and effective thickness $d_{\text{ef}} = (m/m_0)^{1/2}d$] are listed inside for each layer, from the base electrode up.

Figure 5 shows the results of the fitting of the voltage dependence of the specific dynamic conductance $g(V) \equiv A^{-1}dI(V)/dV$ for junctions of both types postannealed at 450 °C. The advantage of fitting the semilog $G(V)$ plots rather than the $\ln I(V)$ curves (Fig. 1) is that in the former case the peculiarities of low-voltage behavior are revealed more clearly—see also Fig. 2. They show, in particular, a minor “cusp” contribution $G_h \propto |V|^{\alpha-1}$ to the conductance (and hence $I_h \propto \text{sgn}(V) \times |V|^\alpha$ to current) similar to that observed and discussed by others—see, e.g., Refs. 46, 49–51. Figure 2 shows that this current component is more sensitive to temperature than the current at higher voltages, though this temperature dependence is still much weaker than that for the Poole-Frenkel conductance mechanism.⁵² Though the exact identification of the physics of the I_h component is beyond the scope of this work, we believe that it is due to a type of hopping (trap-assisted tunneling) strongly affected by the Coulomb interaction of the hopping electrons. In fact, it may be best fitted with the values ($\alpha = 1.8 \pm 0.1$ for Crest 5 and $\alpha = 2.0 \pm 0.3$ for Crest 19) that are relatively close to that of the classical Mott-Gurney law ($\alpha = 2$) for space-charge-limited current.⁵³ A better agreement would be hard to expect, since the Mott-Gurney model implies that the layer thickness d is much larger than the localization radius a of a typical trap, and the thickness of our barriers ($d \sim 2\text{--}3$ nm as

shown below) is comparable with the estimated value $a \sim 1$ nm. For the best fitting, we have subtracted I_h from the data (see the dashed lines in Fig. 5), although the fitting results are appropriate even for the raw data.

As Fig. 5 shows, a relatively good fitting of the data may be achieved with the traditional trapezoidal (i.e., one-layer) model of the barrier. However, better fitting is provided by the potential profile approximation with two (for Crest 5) or three (for Crest 19) linear pieces, implying a layered structure of the oxide. This is not too surprising, since the complex interface chemistry, as well as trapped charge impurities (see, e.g., Ref. 54) may provide interfacial layers with properties different from the oxide bulk. Note that while the I - V curve fitting gives very definite results for the effective thickness $d_{\text{ef}} = (m/m_0)^{1/2}d$ of the layers, it cannot distinguish the contributions to d_{ef} from the effective mass m of the tunneling electron and from the physical thickness d of the barrier.⁵⁵

In order to estimate d (and hence m), we have used measurements of specific capacitance C_0 of the annealed junctions. The specific capacitance has turned out to be close to $2.8 \pm 0.7 \mu\text{F}/\text{cm}^2$ for Crest 5 and $2.3 \pm 0.5 \mu\text{F}/\text{cm}^2$ for Crest 19. Assuming that the dielectric constant of the aluminum oxides is within the range 9 ± 1 (cited in most publications), the capacitance values imply that the physical thickness of oxides is 2.85 ± 0.75 nm for the thermal growth and 3.45 ± 0.85 nm for the plasma oxidation. These estimates have been confirmed using high-resolution transmission electron microscopy (HRTEM). For example, Fig. 3 shows two images of a representative Crest 5 junction annealed at 450 °C. The picture quality is affected by the fact that the base Nb electrode is relatively thick and polycrystalline, so its surface is uneven at a few-nm scale. Nevertheless, the images reveal an amorphous AlO_x layer with a thickness of ~ 3 nm, i.e., reasonably close to that extracted from capacitance measurements.

Using the effective thickness determined by our fitting procedure (see Fig. 5) we estimate the effective mass ($0.35 \pm 0.20m_0$ for the thermally grown oxide and $(0.55 \pm 0.25)m_0$ for the plasma-grown oxide). These values are in a reasonable agreement with the theoretical result $0.4m_0$ of Ref. 56, but substantially lower than the value $\sim 1.0m_0$, which may be deduced from the experimental results of Ref. 57, assuming that the average barrier height for those films (thermally grown with UV stimulation and then annealed at 250 °C) is the same as for our thermally grown layers annealed at the similar temperature. (Probably, the reason of the discrepancy is that the above assumption is incorrect, i.e., that the UV stimulation increases the barrier height substantially.)

We have applied the fitting procedure described above to extract the average barrier height for both as-grown and post-annealed aluminum oxides. We found that the average barrier height $\langle U \rangle$ of the thermally grown oxide increases rapidly at annealing temperatures above 300 °C: from an initial value of ~ 1.8 eV (Ref. 22) to ~ 2.45 eV, and remains close to this value for all the higher annealing temperatures we have explored (up to ~ 550 °C). On the other hand, the average barrier height of the plasma-grown oxide remains practically

unchanged at around 2 eV. Semiquantitatively, this is directly visible from the high- V experimental data shown in Fig. 1, since the barrier height (expressed in electron volts) is always close²⁰ to the voltage of the maximum positive curvature of semilogarithmic plots $\ln I$ vs V , corresponding to the crossover between tunneling through the barrier as a whole at lower voltages, and the Fowler-Nordheim tunneling through its unsuppressed part at higher V .

IV. DISCUSSION

The main result of our experiments is that the average barrier height for thermally grown aluminum oxide layers, postannealed at temperatures close to 450 °C, is substantially (by ~25%) higher than that in the plasma-grown layers. At this stage we do not have a unique explanation of this fact that could be reliably confirmed by experimental facts. However, in the light of the recent experimental X-ray Photoelectron Spectroscopy (XPS) studies^{59,60} and theoretical analysis⁶¹ of aluminum oxidation at various temperatures, the following picture seems most plausible.

The oxides formed by both methods at relatively low temperatures (below ~300 °C) are amorphous,⁶⁰ while their rapid thermal annealing should lead to their gradual ordering, eventually leading to the formation of Al_2O_3 nanocrystals (as in the case of high temperature oxidation^{59,60}). There is an experimental and theoretical evidence⁵⁹⁻⁶¹ that the amorphous phase is more stable at the metal/oxide interfaces; hence one can expect that the crystallization, leading to higher tunnel barrier, starts first in the middle of the barrier. This fact is supported by the fact that the barrier profiles giving the best fits for our tunneling data have a peak in the middle—see inserts on Fig. 5. One may expect the gradual crystallization to depend on the initial state of the oxide. In particular, since the plasma oxide is formed in a more agitated atomic environment, it should be more thermodynamically stable than the thermal oxide. As a result, its transformation into Al_2O_3 should happen at higher temperatures (or, possibly, at much longer annealing at the same temperature—the possibility that we have not yet explored).

Regardless of the reason underlying the different annealing behavior of the thermal and plasma oxides, this fact offers the possibility of using these materials in layered (e.g., “crested”) barriers for advanced floating-gate memories and other applications.¹ Figure 6 shows the tunnel current density $J \equiv I/A$ and the corresponding time scale τ of floating gate recharging calculated for two promising layer combinations: (i) thermal oxide similar to annealed Crest 5, plus plasma oxide similar to Crest 19, and (ii) 1.25-nm SiO_2 layer, plus AlO_x layer similar to Crest 19.

The plots show that the all-aluminum layered barrier of type (i) may sustain the 10-year retention time (standard for nonvolatile memories) at voltages below 1.5 V, while the voltage increase to ~4 V (i.e., by a factor less than 3, enabling a simple NOR structure of memory blocks⁵) would cause the gate recharging in ~10 μs . Such write/erase time is still too long for RAM applications. Note, however, that the voltage applied to each of the layers would be below 2.2 V, ensuring high endurance: charge-to-breakdown well above

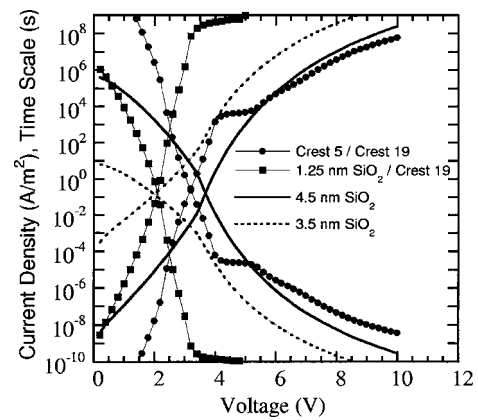


FIG. 6. Tunnel current density $J = I/A$ (increasing with the applied voltage V) and the recharging time constant $\tau \equiv C_0 V/J(V)$ (decreasing with voltage) for two layered tunnel barriers and two uniform SiO_2 barriers, calculated using the aluminum oxide parameters shown in the inset of Fig. 5 and for silicon dioxide parameters taken from Ref. 48 ($U = 3.34$ eV, $m/m_0 = 0.35$). The used dielectric constant values are 10 and 3.9, respectively.

10^5 C/cm², corresponding to more than 10^6 rewrite cycles. This option may be attractive for low-voltage flash memories, especially because there are good prospects of increasing the barrier endurance even further by using higher post-annealing temperatures⁵⁸ and/or Zr alloying of the barriers.⁶²

The results for option (ii), i.e., $\text{SiO}_2/\text{AlO}_x$ barriers, are even more interesting. At $V = 3.2$ V (or higher) such a barrier would allow the floating gate to recharge in less than 1 ns, with voltage about 1.6 V across each layer. For electric fields that are so low, we could not even measure the charge-to-breakdown experimentally, but a simple extrapolation of the high- V data gives an estimate of ~ 10^{15} C/cm², corresponding to ~ 10^{11} rewriting cycles, which are sufficient for RAM applications. The drawback of these barriers would be a relatively short retention time (~100 s at 1.5 V). Too short for nonvolatile memories, this time is still sufficiently long for DRAM-like memories with periodic refresh.

These estimates should be, of course, looked upon with caution, since the calculations shown in Fig. 6 imply that the two layers, which had been grown and measured separately in our experiments, may be combined without a substantial change of their properties. It is more probable that the sequential deposition of the layers will cause at least a moderate change of their parameters and, hence, a deviation from these predictions. Note, however, that these changes may be either detrimental or beneficial for the crested barrier properties. Moreover, some barrier parameters (e.g., thickness of the plasma-grown layer) can be easily changed to compensate for undesirable barrier alterations and to improve the crested barriers performance even further.

To summarize, we have found experimental evidence that electron transport through thermally grown or plasma-grown, postannealed ultrathin aluminum oxide layers is dominated by direct tunneling in electric fields up to ~10 MV/cm. The effective height of the corresponding tunneling barriers, within the annealing temperature range from 300 °C to 550 °C, is substantially dependent on whether the layer has been grown by thermal or plasma oxidation. This fact

offers hope for the implementation of layered all- AlO_x and $\text{SiO}_2/\text{AlO}_x$ barriers for advanced floating-gate memories. Our plans are to explore such barriers experimentally in near future.

ACKNOWLEDGMENTS

This work was supported in part by AFOSR. The authors are grateful to Yu. A. Polyakov and X. Wang for technical assistance. Useful discussions with A. Bratkovsky, J. Cosgrove, M. Gribelyuk, M. Gurvitch, E. P. Gusev, and T.-P. Ma are gratefully acknowledged.

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