High-Quality Aluminum-Oxide Tunnel Barriers for Scalable, Floating-Gate Random-Access Memories (FGRAM)

Xueqing Liu, Vijay Patel, Zhongkui Tan, Konstantin K. Likharev, and James E. Lukens

Stony Brook University, Stony Brook, NY 11794-3800, U.S.A.
E-mail: *klikharev@notes.cc.sunysb.edu*

Abstract

We have demonstrated all-metallic tunnel junctions based on rf-plasma-grown aluminum oxide layers, which enable scalable, floating-gate memory cells with 20-ns-scale write time, 1-s-scale retention time, low operating voltage (3.0-3.5 V), and high endurance in high electric fields (up to 10^{11} write cycles). We believe that such memories may be suitable for some (and after some improvement, most) RAM applications.

1. Introduction

In the course of the continuing search for the "perfect" (scalable, non-volatile, random-access) memory, our group had suggested [1, 2] the concept of NOVORAM – a floating-gate memory based on quantum-mechanical tunneling of electrons through specially crafted layered barriers. According to calculations, at the optimum choice of the potential barrier heights (conduction band offsets) of the layers and their dielectric constants κ, the transparency of such "crested" barriers can be changed by more than 16 orders of magnitude by merely doubling the voltage applied to the barrier, i.e. much faster than barriers made of any known uniform insulator.[1] Such high sensitivity would enable a fast and scalable floating-gate RAM with the cell structure shown in Fig. 1 [1]. Its main difference from the usual non-volatile memories is that in order to suppress the barrier deterioration by hot carriers from the MOSFET channel, the Fowler-Nordheim tunneling responsible for write/erase operations is moved to the back of the floating gate, while the gate oxide is kept thick enough to suppress tunneling at all times.

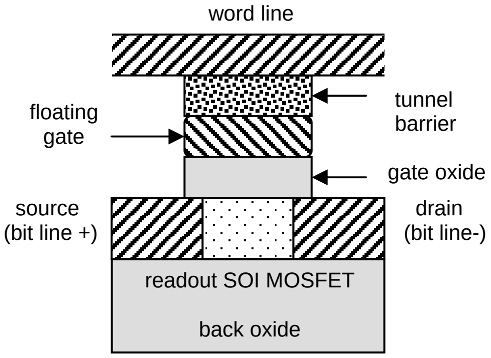

Fig. 1: Memory cell structure of NOVORAM and FGRAM [2].

The later experimental work has shown that layered barriers made of several material combinations (including $Si_3N_4/SiO_2/Si_3N_4$ [4, 5], SiO_2/ZrO_2 [6], $HfON/Si_3N_4$ [7], and SiO_2/AlO_x [8]) can indeed improve the barrier transport sensitivity to voltage in comparison with the traditional SiO_2 barriers. Unfortunately, to the best of our knowledge, the conductivity change ranges demonstrated so far have not been sufficient for the full implementation of the NOVORAM concept. In particular, the attempts by our group to combine different species of aluminum oxide (for example, thermally-grown and plasma grown AlO_x [9]) to form crested barriers so far have not been successful. However, in the course of this work we have found a way to fabricate quasi-uniform aluminum oxide layers with very high transport properties, including high endurance to electric fields in excess of 10 MV/cm, and extremely high values of charge-to-breakdown (close to 10^6 C/cm^2). These properties may be used in what we call Floating-Gate Random-Access Memories (FGRAM) with the cell structure similar to NOVORAM (Fig. 1).[2] Essentially the only difference of the memory operation is the necessity to refresh the FGRAM contents exactly as this is currently done in DRAM. Our AlO_x barriers may provide the retention time (of the order of 1 s) necessary for this operation.

2. Fabrication

The barriers have been fabricated in nearly the same way as those described in Ref. 9. Briefly, thin (10-nm-scale) aluminum films have been dc-sputtered either directly on oxidized silicon wafers or on a sub-layer of a different metal. Immediately after their deposition, the films have been oxidized in an rf plasma discharge, with power from 10 to 250 W at oxygen pressure in the range from 15 to 75 mtorr. (The results shown below correspond to the lower ends of these ranges.) Immediately after the oxidation (without a vacuum break) the junctions have been sealed with a metallic counter-electrode. Such in-situ fabrication results in highly reproducible junctions, with conductivity scaling well with the junction area A (which ranged from 3×3 to 300×300 μm^2). In order to improve the junction quality, in particular their endurance in high electric field, after the lithographic area definition, they have been subjected to rapid thermal post-annealing (RTA) for 10 to 180 seconds at temperatures from 300 to 550°C.

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[1] The difference of κ alone may also provide a transparency steepness improvement [3], though for realistic values of parameters this effect it weaker than that of the tunnel barrier height difference.

[2] This opportunity was briefly mentioned in Ref. 10.

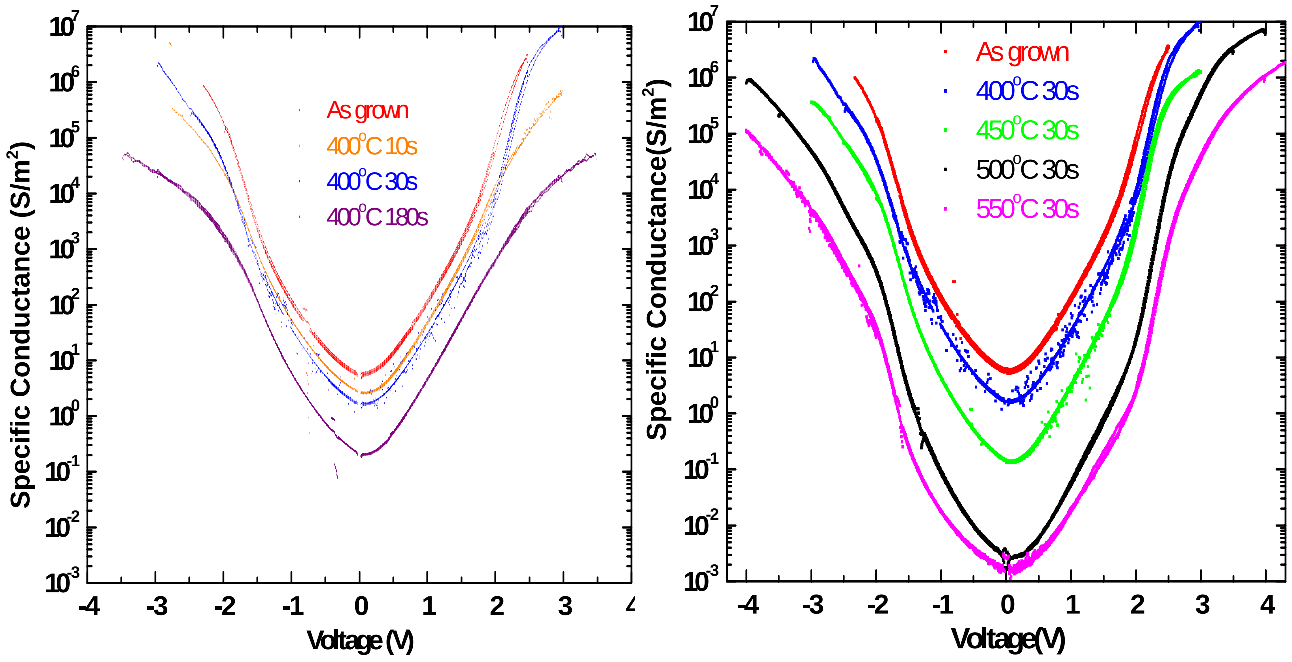

Fig. 2 : Specific differential conductance $G \equiv A^{-1}(dI/dV)$ of junctions from wafer CB17 (rf power 10 W, oxidation time 10 minutes) as a function of applied voltage, for various durations and temperatures of the rapid thermal post-annealing. The data are for $T = 4.2$ K, but the room temperature results are close, with the only exception of somewhat lower breakdown voltage.

3. Experimental results

Throughout this range of fabrication conditions, the junctions show steep *I-V* curves (Fig. 2) with very weak temperature dependence (similar to that shown in Fig. 2 of Ref. 9), which can only be explained by direct tunneling[3] of electrons through the whole AlO_x layer. Moreover, the fitting of the curves with the "microscopic" (non-WKB) theory [9] has shown that the results may be reasonably well described by tunneling through a uniform potential barrier with a height (depending on the exact fabrication parameters) from 2.0 to 2.4 eV and an effective thickness $d_{ef} = (m_{ef}/m_0)^{1/2}d$ from 1.75 to 2.5 nm. The estimates of the effective mass m_{ef} of the carriers using the junction capacitance measurements [9], as well as high-resolution TEM (courtesy by Dr. Y. Zhu, Brookhaven National Laboratory) show that the physical thickness d of the barriers is in reasonable correspondence with d_{ef}, with the ratio m_{ef}/m_0 somewhere between 0.3 and 0.5.

As Fig. 2 shows, the rapid thermal annealing results in a dramatic improvement of the junction endurance to high electric field. In particular it increases the breakdown dc fields above 10 MV/cm at room temperature (and above 15 MV/cm at 4.2K), i.e. substantially beyond those for the best SiO_2 layers we are aware of.

Another striking feature of these junctions is their high charge-to-breakdown Q_{BD} which (for some fabrication parameters) exceeds 10^5 C/cm², the number to be compared with $\sim 10^1$ C/cm² for typical SiO_2 layers used in flash memories. Figure 3 shows a more adequate figure-of-merit, the maximum number of write cycles $N \equiv Q_{BD}/CV$, plotted versus the calculated write time scale $\tau \equiv CV/I(V)$, where C is the junction capacitance (for our samples, between 1.5 and 2.0 μF/cm²), V is the (high) applied voltage, and $I(V)$ the current corresponding to this voltage.

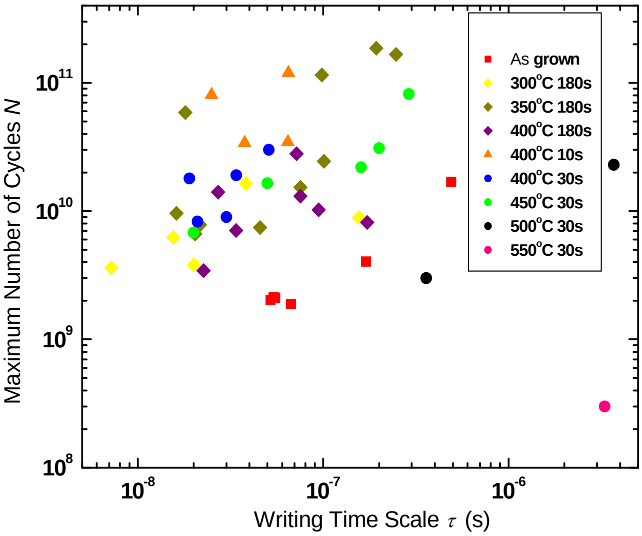

Fig. 3 : Field endurance of junctions from wafer CB17 for several RTA parameter sets, at room temperature.

One can see that at semi-optimized post-processing, the junctions can combine a 20-ns-scale write time (acceptable for most applications currently using stand-alone DRAM chips) with $\sim 10^{11}$ write cycles and ~1-second-scale retention time $\tau_R \equiv C/G(0)$. We believe that these parameters enable the application of FGRAM, based on such tunnel barriers, for at least some RAM

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[3] We use this term to describe all ranges of applied voltage, including the Fowler-Nordheim regime.

applications, though the further increase of N may be still desirable. Our plans are to continue the optimization of fabrication parameters to achieve this goal.

4. Conclusion

To summarize, we have shown that such simple, CMOS-compatible fabrication steps as plasma oxidation of aluminum with rapid thermal post-annealing of the resulting junctions enable the implementation of fast, scalable floating-gate memories which may be suitable for at least some RAM applications. We believe that such memories, after a modest improvement, may become the RAM of choice for integrated circuits beyond the 32-nm ITRS technology node.[4]

5. Acknowledgments

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References

[1] K. Likharev, “Layered tunnel barriers for nonvolatile memory devices”. *Appl. Phys. Lett.*, vol. 73, pp. 2137-2139, Nov. 1998.

[2] K. K. Likharev, “NOVORAM: A new concept for fast, bit-addressable nonvolatile memory based on crested barriers”, *IEEE Circuits and Devices*, vol. 16, pp. 16-21, June 2000.

[3] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Mayer, “VARIOT: A novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices”, *IEEE Electron Dev. Lett.*, vol. 24, pp. 99-101, Feb. 2003.

[4] S. J. Baik , S. Choi, U-I. Chung, and J. T. Moon, “Engineering on tunnel barrier and dot surface in Si nanocrystal memories”, *Solid-State Electronics*, vol. 48, pp. 1475–1481, Sep. 2004.

[5] S. H. Hong, J. H. Jang, T. J. Park, D. S. Jeong, M. Kim, C. S. Hwang, and J. Y. Won, “Improvement of the current-voltage characteristics of a tunneling dielectric by adopting a Si_3N_4 /SiO_2/Si_3N_4 multilayer for flash memory application”, *Appl. Phys. Lett.,* vol. 87, art. 152106, Oct. 2005.

[6] B. Govoreanu, P. Blomme, J. Van Houdt, and K. De Meyer, “Enhanced tunneling current effect for nonvolatile memory applications”, *Jpn. J. Appl. Phys.*, *Part 1*, vol. 42, pp. 2020–2024, Apr. 2003.

[7] Y. Liu, S. I. Shim, F. C. Yeh, X. W. Wang, and T. P. Ma, “Barrier engineering for non-volatile memory application”, Report 3.2 at *SISC 2006* (San Diego, CA, December 2006), and to be published.

[8] J. Cosgrove, private communication (2006).

[9] E. Cimpoiasu, S. K. Tolpygo, X. Liu, N. Simonian, J. E. Lukens, K. K. Likharev, R. F. Klie and Y. Zhu, “Aluminum oxide layers as possible components for layered tunnel barriers”, *J. Appl. Phys.*, vol. 96, pp. 1085-1093, July 2004.

[10] K. K. Likharev, “Electronics below 10 nm”, in: J. Greer *et al.* (eds.), *Nano and Giga Challenges in Microelectronics*, Elsevier, Amsterdam, 2003, pp. 27-68.

[11] J. C. Scott, “Is there an immortal memory?”, *Science*, vol. 304, pp. 62-63, Apr. 2004.

[12] D. B. Strukov and K. K. Likharev, “Defect-tolerant architectures for nanoelectronic crossbar memories”, *J. of Nanoscience and Nanotechnology*, vol. 7, pp. 151-167, Jan. 200

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[4] Their main competition may be resistive memories [11] with their more compact memory cells ($4F^2$ vs. $6F^2$), especially in their hybrid (“CMOL”) version [12].